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Electronics Design Checklist

This document was adapted with permission from Electronics Design Checklist by Hank Wallace, ChipCentre Guides & Experts, Electronics Design, EE Expert Hank Wallace, http://archive.chipcenter.com/eexpert/hwallace/hwallace001.html (accessed 2010-10-08).

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Electronic and Schematics

1. All unused inputs terminated
2. Race conditions checked
3. Darlington outputs (1.2v low) driving logic inputs
4. Mating connectors on different assemblies checked for same pinout
5. All outside world I/O lines filtered for RFI
6. All outside world I/O lines protected against static discharge
7. Bypass cap for each IC
8. Voltage ratings of components checked
9. Ensure 3.3 volt parts are 5 volt tolerant where they interface
10. Verify power sequencing requirements on 5 volt and 3.3 volt rails
11. Each IC has predictable or controlled power-up state
12. File name on each sheet
13. Dot on each connection
14. Minimum number of characters in values
15. Consistent character size for readability
16. Schematics printed at a readable scale
17. All components have reference designators and values
18. Special PCB or parts list information entered for each component, if required
19. Polarized components checked
20. Electrolytic and tantalum capacitors checked for no reverse voltage
21. Power and ground pins listed for each component with hidden power pins
22. Check hidden power and ground connections
23. Title block completed for each sheet
24. Ground made first and breaks last for hot pluggability
25. Pull-ups on all open collector outputs
26. Separate pullup/pulldown resistors on all mode pins to allow modes to be changed if needed
27. Sufficient power rails for analog circuits

28. LM324 and LM358 outputs loaded to prevent crossover distortion
29. Amplifiers checked for stability
30. Oscillators checked for reliable startup
31. Consider signal rate-of-rise and fall for noise radiation
32. Check for input voltages applied with power off and CMOS latchup possibilities
33. Reset circuit design reliable, both glitch-free and consistent; tested with fast and slow power supply rise and fall time
34. Check reset behavior if power cycles before the circuit is fully operational
35. For synchronous resets be sure the circuit can withstand unknown outputs until the clock starts
36. Check all resets for possible reset loops, especially for designs that are hot swap capable
37. Separate analog signals from noisy or digital signals
38. Ability to disable watchdog timer for testing and diagnostics and emulation
39. Sufficient capacitance on low dropout voltage regulators
40. Setup, hold, access times for data and address busses
41. Capacitance and fan out limits checked for busses
42. Check the data sheet fine print and apnotes for weird IC behaviors
43. Determine effect of losing each of multiple grounds on a connector
44. Automotive powered devices must withstand 60 to 100 volt surges
45. Check maximum power dissipation at worst-case operating temperatures
46. Check time delays and slew rates of opamps used as comparators
47. Check opamp input over-drive response for unintended output inversion
48. Check common mode input voltages on opamps
49. Check for voltage transients and high voltages on FET gates
50. Check failure modes and effects of failed power semiconductors
51. Estimate total worst case power supply current
52. Check pin numbers of all custom-generated parts
53. Pinout may vary between DIP and various SMD packages; library parts may not match the intended package
54. For buses, ensure bus order matches device order
55. Ensure resistors are operating within their specified power range plus safety factor
56. Resistor power ratings derated for elevated ambient temperatures
57. Electrolytic/tantalum capacitor temperature/voltage derating sufficient for MTBF
58. Check for low impedance sources driving tantalum caps which can cause premature failure
59. Avoid reverse base-emitter current/voltage on bipolar transistors
60. Check PLD pinouts each time a PLD is recompiled

61. Preferred component reference designators
    - R fixed resistor
    - RN resistor network
    - RV variable resistor
    - C capacitor (network, fixed or variable)
    - L inductor
    - Q transistor, FET, SCR, TRIAC
    - D, CR diode, rectifier, Zener, varicap, LED
    - DL multi-segment display (any type)
    - VR, Q, IC voltage regulator
    - U, IC integrated circuit
    - J socket, jack (female) OR the half that is stationary
    - P plug (male) OR the half that is attached to a cable/wire
    - JP jumper (pins, trace, or wire)
    - Y, X crystal
    - M modular subassembly, daughter board
    - S mechanical switch
    - F fuse
    - FL filter
    - T transformer
    - KB keyboard
    - B, BT battery

PCB Design

1. Hole dia on drawing are finished sizes, after plating
2. Finished hole sizes are >=10 mils larger than lead, or larger spec dictated by automatic insertion gear
3. Silkscreen legend text weight >=10 mils
4. Pads >=15 mils larger than finished hole sizes
5. Place thruhole components on 50 mil grid
6. No silkscreen legend text over vias (if vias not soldermasked) or holes
7. Soldermask does or does not cover vias
8. All legend text reads in one or two directions
9. Components labeled left-right, top-bottom
10. Company logo in silkscreen legend
11. Company logo in foil
12. Copyright notice on PCB

13. Date code on PCB
14. Compliance notice on PCB (e.g. UL flammability rating)
15. PCB part number and layer number on each layer in copper
16. Assembly part number on PCB
17. All polarized components point same way
18. Components >=0.2" from edge of PCB
19. Ground planes where possible
20. Test pad or test via on every net to allow in circuit test
21. For in-circuit test, no logic pins connected directly to power or ground
22. Test point on all unused outputs for use in debug
23. Test pads 200 mils from edge of board
24. Mounting holes electrically isolated or not
25. Mounting holes with or without islands
26. Proper mounting hole clearance for hardware
27. All polarized components checked
28. No acute inside angles in foil
29. Traces >= 20 mils from edge of PCB
30. PCB revision on silkscreen legend
31. Assembly revision blank on silkscreen legend
32. Serial number blank on silkscreen legend
33. Soldermask swell checked
34. Thru-hole drill tolerance noted
35. Thru-hole soldermask tolerance noted
36. Thru-hole route tolerance noted
37. Thru-hole silkscreen legend tolerance noted
38. Drill legend shows all symbols and sizes
39. Mounting holes matched 1:1 with mating parts
40. Automated netlist check
41. Manual netlist check
42. Check netlist for nodes with only one connection
43. All nets have meaningful names with modifiers for signal polarity, differential signals, busses
44. Net names case insensitive, alphanumeric, name length compatible with other tools
45. Beware a net named NC
46. Verify that nodes in a netlist with more than N connections are valid
47. CAD design rule check
48. Drill origin is a tooling hole
49. Checkplots sent with disk based photoplot files

50. NC drill and photoplot file language format noted
51. Tools on drill plot and NC drill file cross checked
52. Soldermask over bare copper noted if needed
53. PCB thickness, material, copper weight noted
54. Trace and space geometry noted
55. Printed drill report sent with checkplots
56. Printed aperture table sent with checkplots
57. Photoplot files checked in file viewer
58. Test coupon on PCB containing minimum geometry features
59. Trace width sufficient for current carried
60. Minimum component body spacing
61. SMD pad shapes checked
62. Visual references for automated assembly
63. Tooling holes for automated assembly
64. Tooling and mounting holes have internal plane clearance to avoid multilayer shorts
65. Sufficient clearance for high voltage traces
66. Component and trace keepout areas observed
67. High frequency circuitry precautions observed
68. Thermal reliefs for internal power layers
69. Solder paste mask openings are proper size
70. Blind and buried vias allowed on multilayer PCB
71. PCB layout panelized correctly
72. Panelized PCB fits test and manufacturing equipment
73. Breaking or cutting apart panelized PCBs after loading can stress/crack SMD parts near the break points; place parts away from stress areas
74. Sufficient clearance for socketed ICs
75. SMD component orientation arbitrary or consistent
76. Ensure pin 1 interpretation and orientation consistent among all connectors of a given type on the board
77. Clearance for IC extraction tools
78. Clearance for emulator adapter
79. Clearance for sockets for ICs during proto phase
80. Standoffs on power resistors or other hot components
81. Digital and analog signal commons joined at only one point
82. EMI and RFI filtering as close as possible to exit and entry points in shielded areas
83. Layout PCB so that any rework or repair of a component does not require removal of other components
84. Extra connector and IC pins accessible on prototype boards, just in case

85. Check all power and ground connections to ICs
86. Provide ground test points, accessible and sized for scope ground clip
87. Potentiometers should increase controlled quantity clockwise
88. Check hole diameters for odd components: rectangular pins, spring pins
89. Check the orientation of all connectors using actual connector/cable
90. Bypass capacitors located close to IC power pins
91. All silkscreen text located to be readable when the board is populated
92. All ICs have pin one clearly marked, visible even when chip is installed
93. High pin count ICs and connectors have corner pins numbered for ease of location
94. Silk screen tick marks for every 5th or 10th pin on high pin count ICs and connectors
95. Verify that all series terminators are located near the source
96. Place I/O drivers near where their signals leave the board
97. High frequency crystal cases should be flush to the PCB and grounded
98. Check for traces running under noisy or sensitive components
99. Check IC pin count on layout vs schematic
100. No vias under metal-film resistors and similar poorly insulated parts
101. Check for traces which may be susceptible to solder bridging
102. Maximize distances between features where possible
103. Check for dead-end traces
104. Check for PWR not shorted to GND
105. Ensure schematic software did / did not separate Vcc from Vdd, Vss from GND as needed
106. Provide multiple vias for high current and/or low impedance traces

PCB Assemblies

1. Miscellaneous parts on bill of materials and assembly notes for same: hardware, heat sinks, heat sink compound or composite insulators, IC sockets, consumables
2. Assembly notes for all special operations
3. Conformal coating
4. Special static handling precautions required during assembly and test

Wired Assemblies

1. Wire gauge checked for compatibility with each termination
2. Cable ties or lacing cord shown where needed
3. Length and color of each wire indicated
4. Check voltage drop at maximum current with specified gauge and length for entire current path (eg. power and ground)
5. Notes about application of wire terminations (technique, heat shrink tubing, amount of solder, crimp force, tools, etc.)

Parts Lists

1. Each component has quantity, reference designator and description
2. List qualified part numbers for special devices
3. Suggested and alternate manufacturer(s) listed
4. Object/binary code and method/programmer specified for each programmable device
5. Price and availability checked for each component

Mechanical Drawings

1. Standard title block and border used
2. No dimensions on the material
3. Every feature must have X and Y dimension, along with radius, diameter, etc.
4. Every hole must be checked for alignment with mating hole(s) in other parts
5. Check every hole diameter
6. Tolerance for sheet metal feature position noted
7. Tolerance for sheet metal hole size noted
8. Specify material
9. Specify finish
10. Specify units
11. Specify debur or brush
12. Details for special operations
13. File name on each sheet
14. CAD layers shown on drawing
15. All hardware specified and listed on parts list
16. Screw lengths checked; extra thread required for fasteners (nut, lockwasher, washer)
17. Hole diameters checked for each screw
18. Tapped hole thread details indicated

Software

1. Each version archived for future reference
2. Loops checked for terminating conditions
3. Communications timeouts checked
4. All branches tested
5. Revision history noted for all changes
6. CPU utilization measured
7. Interrupt response time measured
8. Interrupt execution time measured
9. Naming conventions consistent and relevant to humans

10. Adherence to coding style standards
11. Power-up, power-down considerations
12. Unused vectors trapped to restart or damage control routine
13. Unused ROM space loaded with trap or restart instructions
14. Warm and cold reset differences
15. Non-volatile memory corruption possibilities checked during power-up, power-down, and program-gone-wild conditions
16. Design notes within or separate from code
17. Check for FIFO and buffer overruns
18. Check critical timer driver code
19. Check for odd address usage on 16/32 bit micros, especially an odd stack pointer
20. Use a LINT utility on C programs to find subtle problems
21. Program's data structures contain version numbers to detect program version upgrades and translate the structures' formats

Testability

1. Test points on PCBs for critical circuits, hard to reach nets
2. Test pads for in-circuit or bed-of-nails functional testing
3. Test pads on a regular grid
4. Test procedure written for each test phase
5. Special test arrangements and connectors for testing

Maintainability

1. Easy disassembly and reassembly
2. Fuses accessible and labeled
3. Self test mode
4. Spare parts available
5. Status LEDs on PCB
6. Event logging of exceptional conditions
7. Vibration tolerance of entire assembly and individual modules
8. Surge current magnitude through semiconductors within rating
9. Thermal cycling excursions internal to components and assemblies within acceptable limits
10. Capacitors mounted below or away from heat-dissipating devices such as transformers
11. Resistance and tolerance of entire product to static discharge via any path

Safety

1. Fuse and circuit breaker size and characteristics
2. Fuse sizes marked near fuse holder
3. Room to remove fuse without damaging other components
4. Spare fuse storage
5. Shock hazards
6. Radiated energy warnings and shields
7. Applicable standards checked
8. Protection against liquids and foreign objects

Documentation

1. End-user instructions: unpacking, how to use, warranty, service, troubleshooting
2. Service manual: troubleshooting procedures, parts lists, helpline info
3. Design notes: why were significant design decisions made the way they were
4. Other info that may be lost if designers depart the organization
5. Electronics Design Archive